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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,185	11/11/2003	Paul A. Farrar	303.367US3	4652
21186	7590	07/06/2005	EXAMINER	
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. BOX 2938 MINNEAPOLIS, MN 55402-0938			NADAV, ORI	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 07/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Advisory Action
Before the Filing of an Appeal Brief**

Application No.

10/705,185

Applicant(s)

FARRAR ET AL.

Examiner

Ori Nadav

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--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 22 June 2005 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
(a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
(b) ☐ They raise the issue of new matter (see NOTE below);
(c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
(d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
The status of the claim(s) is (or will be) as follows:
Claim(s) allowed: _____.
Claim(s) objected to: _____.
Claim(s) rejected: _____.
Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:
See attachment.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____.
13. ☐ Other: _____.



ORI NADAV
PRIMARY EXAMINER

Response to Arguments

Applicant argues that there is support and adequate description for the claimed limitations of a capacitor and a plurality of substantially parallel buried conductive elements, as recited in claim 1, and for a first buried layer and the second buried layer being substantially parallel to the active semiconductor layer, as recited in claim 9, because the disclosure recites a capacitor and two buried conductive elements lines 114 (page 5, lines 27 and 29), and figure 1b depicts a first buried layer and the second buried layer being substantially parallel to the active semiconductor layer.

The examiner agrees that the disclosure recites a capacitor and two buried conductive elements lines 114, as applied to the embodiment of figure 1b. However, there is no support and adequate description for the claimed limitations of a capacitor and a plurality of substantially parallel buried conductive elements, as recited in claim 1, and for first buried layer and the second buried layer being substantially parallel to the active semiconductor layer, as recited in claim 9. Furthermore, figure 1b does not depict a first buried layer and the second buried layer being substantially parallel to the active semiconductor layer.

Applicant argues that there is support and adequate description for the claimed limitations as recited in claims 2, 4, 11 and 18-19, because the general description in the disclosure can apply to the embodiment of figure 1b.

The examiner agrees that the general description in the disclosure can apply to the embodiment of figure 1b. Therefore the objection to the specification and the 112 rejection are being withdrawn.

Applicant argues that there is support and adequate description for the claimed limitations as recited in claims 8 and 15, because the embodiment of figure 1b recites that it might have an additional level of buried elements.

The recitation that the embodiment of figure 1b recites might have an additional level of buried elements does not provide support and adequate description for the claimed limitations of a second buried layer including a plurality of substantially parallel second conductive elements oriented in a second direction, a second depth being greater than the first depth, and a deep trench capacitor formed between the plurality of substantially parallel first conductive elements, as recited in claims 8 and 15. Furthermore, the disclosure recites in page 6, line 5, that an alternative embodiment to that of figure 1b might have an additional level of buried elements. Clearly, this is an alternative embodiment to that of figure 1b, and not the elected embodiment of figure 1b.

Applicant argues that there is support and adequate description for plurality of substantially parallel second conductive elements located either in front of or behind the deep trench capacitor, as recited in claim 15, because the embodiment of figure 1b

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recites in page 6, line 5, that it might have plurality of substantially parallel second conductive elements located either in front of or behind the deep trench capacitor.

The disclosure recites in page 6, line 5, that an alternative embodiment to that of figure 1b might have plurality of substantially parallel second conductive elements located either in front of or behind the deep trench capacitor. Clearly, this is an alternative embodiment to that of figure 1b, and not the elected embodiment of figure 1b.

Applicant argues that there is support and adequate description for the claimed limitations as recited in claims 2, 4, 11 and 18, because the general description in the disclosure can apply to the embodiment of figure 1b.

Although it is conventional to use a device comprising a capacitor and an active device layer as a DRAM, it is not conventional to use a device comprising a capacitor and an active device layer as, for example, a flash memory. Therefore, there is no support and adequate description for the claimed limitations which include integrated circuits adapted for use with at least one of the group consisting of: dynamic random-access memory (DRAM), static random-access-memory (SRAM), flash memory, synchronous dynamic random-access-memory (SDRAM), extended-data-out random-access-memory (EDO RAM), and burst-extended-data-out random-access-memory (BEDO RAM), as recited in claim 16.

Applicant argues that Okumura does not teach in figures 6 and 7 and related text a semiconductor device comprising a doped silicon substrate having an active semiconductor layer formed thereon, and a conductive element separated from the active semiconductor layer by and surrounded by an oxide insulating material, because semiconductor layer 9 is a word line and not an active semiconductor layer, the conductive element 1 is a polysilicon bit line, that layer 24 is the gate oxide of the transistor formed by diffusions 4 and 2 with the word line 9 as the gate electrode and not an isolation oxide as claimed, and that the poly bit line is not surrounded by the oxide insulating materials as claimed by the examiner, but is in direct contact with the diffused source/drain region 2.

The fact that semiconductor layer 9 is a word line, that conductive element 1 is a polysilicon bit line, that layer 24 is the gate oxide of the transistor and that the poly bit line is in direct contact with the diffused source/drain region 2, does not mean that Okumura does not teach in figures 6 and 7 and related text a semiconductor device comprising a doped silicon substrate having an active semiconductor layer formed thereon, and a conductive element separated from the active semiconductor layer by and surrounded by an oxide insulating material, as claimed. Note that although the bit line is in direct contact with the diffused source/drain region 2, the bit line is still surrounded by the oxide insulating materials 24, 10b and 14.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



O.N.
6/29/05

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TECHNOLOGY CENTER 2800